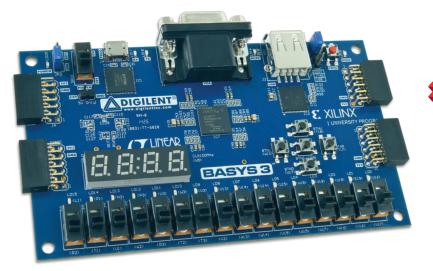
BASYS 3

Portal to the Vivado® Design Suite, powered by the Artix-7™





The Basys3 is an entry-level FPGA board designed exclusively for the Vivado Design Suite, featuring Xilinx Artix 7-FPGA architecture. Basys3 is the newest addition to the popular Basys line of starter FPGA boards. Basys3 includes the standard features found on all Basys boards: complete ready-to-use hardware, a large collection of on-board I/O devices, all required FPGA support circuits, and a free version of development tools and at a student-level price point.

Now with the Basys3, Digilent gives students a better representation of professional-level engineering by greatly improving the feature sets. These improvements include:

More I/O:

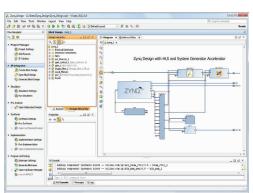
Double the user interface switches, double the number of onboard outputs, upgraded the number of external ports (moving from 6-pin single-row Pmods to 12-pin double-row Pmods) and included for the first time on a Basys class device a USB-UART bridge.

Modern Architecture = Modern Programming Challenges:

Due to the migration from the Spartan 3E family to the Artix-7 class of device, the Basys3 offers a substantial increase in hardware capabilities. With the new Artix FPGA comes 15X the logic cells (from 2,160 to 33,280) and the upgrade from multipliers to true DSP slices. It also adds over 26X the amount of RAM.

Industry's First SOC Strength Design Suite:

The most significant change to the Basys3 is the upgrade to Xilinx Vivado Design Suite, the most modern design tool chain used by professional engineers worldwide. Compared to ISE, Vivado offers an improved user experience and expanded capabilities. These capabilities include block based IP integration (which can reduce development time up to 10x) and the Vivado Logic/Serial I/O analyzer.



Features the Artix-7 (XC7A35T-1CPG236C):

- 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops)
- 1,800 Kbits of fast block RAM
- Five clock management tiles, each with a phase-locked loop (PLL)
- 90 DSP slices
- Internal clock speeds exceeding 450MHz
- On-chip analog-to-digital converter (XADC)

The Basys3 offers an expansive lineup of ports and peripherals to introduce system-level design concepts:

- 16 user switches
- 16 user LEDs
- 5 user pushbuttons
- 4-digit 7-segment display
- 4 Pmod connectors
- 3 Standard 12 pin Pmod 1 dual purpose XADC signal/ standard Pmod
- 12-bit VGA output
- USB-UART Bridge
- Serial Flash
- Digilent USB-JTAG port for FPGA programming and communication
- USB HID Host for mice, keyboards and memory sticks



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